

A large, stylized logo for the 65xx series, featuring the text '65xx' in red with a blue shadow effect, set against a light blue oval background.

W65C816SXB
Engineering Development System
Datasheet

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DOCUMENT REVISION HISTORY

| Version | Date | Author | Description |
|---------|-----------|------------|---|
| 0.1 | 1-Jun-13 | David Gray | Initial Document Entry |
| 0.2 | 06-Jun-14 | David Gray | Updated Quick Reference Guide and Added Ordering section. |
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Contents

- DOCUMENT REVISION HISTORY 2
- 1. Introduction and Features 4
 - 1.1 Feature List..... 4
 - 1.2 Functional Block Diagram 4
 - 1.3 Board Diagram..... 5
 - 1.4 W65C816SXB QUICK REFERENCE GUIDE 6
- 2. Connector Descriptions 8
 - 2.1 XBus Port (J1) 8
 - 2.2 PIA Port (J2)..... 8
 - 2.3 VIA Port (J3)..... 8
 - 2.4 ACIA Port (J4) 8
 - 2.5 USB TIDE Port (J5)..... 8



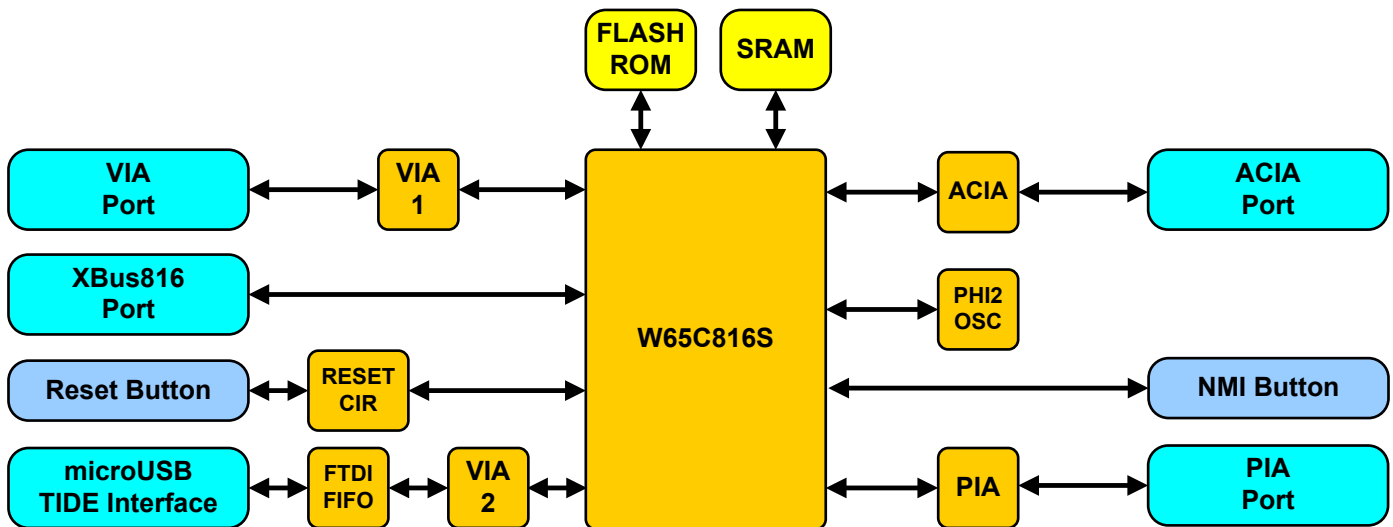
1. Introduction and Features

The W65C816SXB is an educational and industrial strength Engineering Development System based around the world renowned W65C816S 8-bit microprocessor. With its vast I/O provided by the on board W65C22 VIA, W65C21 PIA, and W65C51 ACIA peripheral ports the 816SXB provides the user with easy access to the vast flexibility in design possibilities using our Addressable Register Architecture (ARA). The addition of the XBus allows for expansion beyond the standard on board peripherals by providing full Data Bus, Address Bus and Control Signal access.

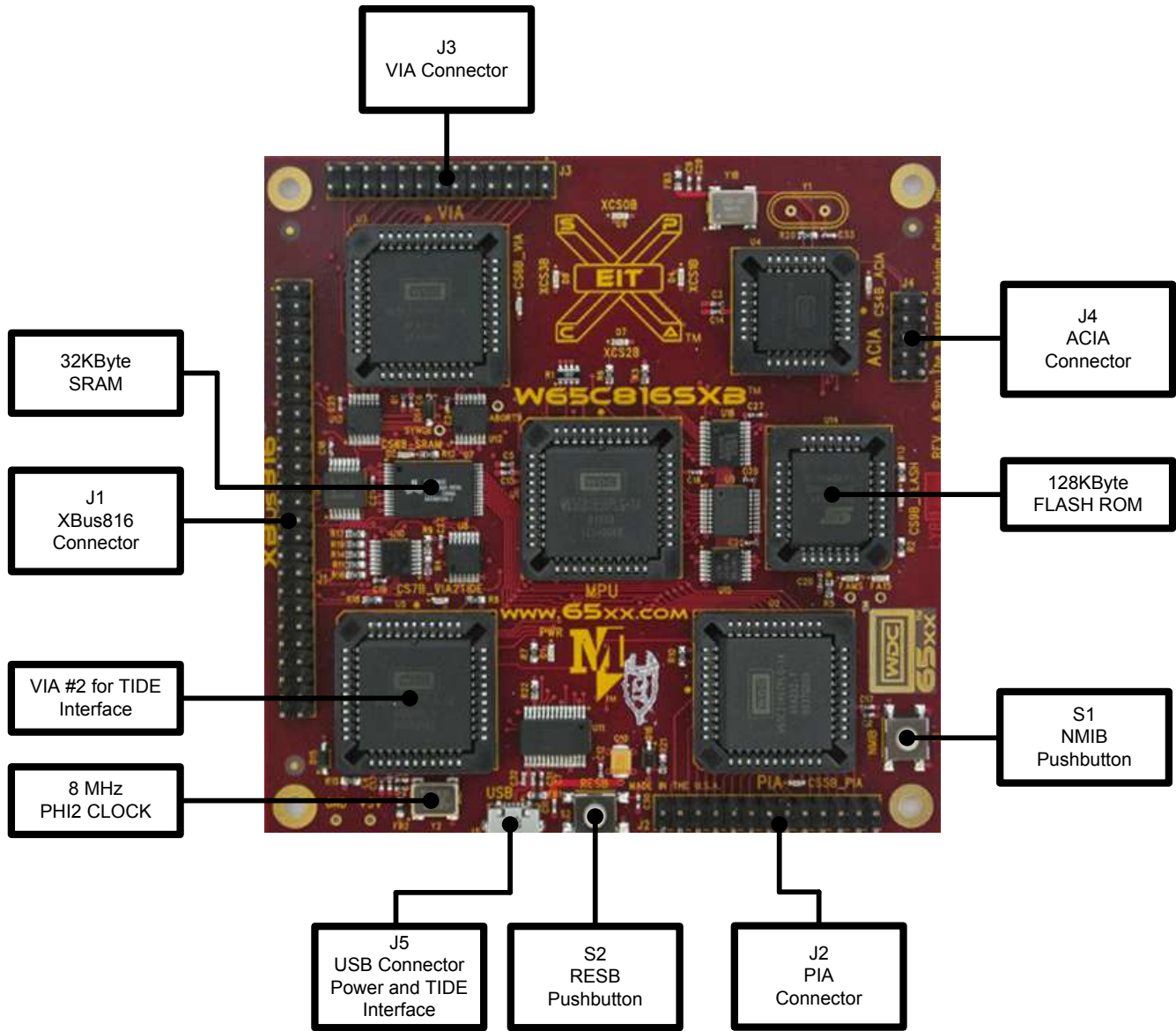
1.1 Feature List

- W65C816S MPU running at 8MHz. Refer to the [W65C816S Datasheet](#) for details on the processor.
- 2 x W65C22N VIA(1/2) - One for USB FIFO Interface and one VIA Expansion Port
- 1 x W65C21 PIA with PIA Expansion Port
- 1 x W65C51N ACIA with ACIA Expansion Port
- 1 x XBus816 Connector with full address, data and control lines of the processor and 3 external chip selects
- 1 x 128Kbytes FLASH ROM (32PLCC Socket) mapped as upper 32KB of Memory Map with overlays off of 2 IO pins from W65C22 TIDE (VIA2) Port
- 1 x 32Kbytes SRAM
- Programming/Debug Interface – FTDI245 FIFO connected to VIA2 (W65C22N) using the onboard ROM Monitor.
- Micro USB Connector – USB Power and Debugging Interface

1.2 Functional Block Diagram



1.3 Board Diagram



100mm x 100mm PCB



1.4 Quick Reference Guide – Memory Map

| <i>W65C816SXB Memory Map</i> | | | | |
|------------------------------|------------|-------------|--------------------|---|
| <i>Start</i> | <i>End</i> | <i>Size</i> | <i>Chip Select</i> | <i>Description</i> |
| 0x8000 | 0xFFFF | 32 KB | CS9B | FLASH ROM (x4, 128KB used with 2 IO pins for overlays) |
| 0x0000 | 0x7FFF | 32 KB | CS8B | SRAM (7FFF-7F00 is Decoded for expansion) |
| 0x7FE0 | 0x7FFF | 32 B | CS7B | VIA-TIDE |
| 0x7FC0 | 0x7FDF | 32 B | CS6B | VIA Port |
| 0x7FA0 | 0x7FBF | 32 B | CS5B | PIA Port |
| 0x7F80 | 0x7F9F | 32 B | CS4B | ACIA Port |
| 0x7F60 | 0x7F7F | 32 B | XCS3B | XBus Chip Select 3 |
| 0x7F40 | 0x7F5F | 32 B | XCS2B | XBus Chip Select 2 |
| 0x7F20 | 0x7F3F | 32 B | XCS1B | XBus Chip Select 1 |
| 0x7F00 | 0x7F1F | 32 B | XCS0B | XBus Chip Select 0 |



1.5 Quick Reference Guide – Expansion Connectors

| <i>J1 – XBus816 Connector</i> | | | |
|-------------------------------|--------------------|------------|--------------------|
| <i>Pin</i> | <i>Signal Name</i> | <i>Pin</i> | <i>Signal Name</i> |
| 1 | VDD | 2 | VSS |
| 3 | D0 | 4 | D1 |
| 5 | D2 | 6 | D3 |
| 7 | D4 | 8 | D5 |
| 9 | D6 | 10 | D7 |
| 11 | A0 | 12 | A1 |
| 13 | A2 | 14 | A3 |
| 15 | A4 | 16 | A5 |
| 17 | A6 | 18 | A7 |
| 19 | A8 | 20 | A9 |
| 21 | A10 | 22 | A11 |
| 23 | A12 | 24 | A13 |
| 25 | A14 | 26 | A15 |
| 27 | A16 | 28 | A17 |
| 29 | A18 | 30 | A19 |
| 31 | A20 | 32 | A21 |
| 33 | A22 | 34 | A23 |
| 35 | XCS0B | 36 | XCS1B |
| 37 | XCS2B | 38 | XCS3B |
| 39 | VPB | 40 | IRQB |
| 41 | NMIB | 42 | RESB |
| 43 | MLB | 44 | VDA |
| 45 | VPA | 46 | BE |
| 47 | RWB | 48 | PHI2 |
| 49 | VSS | 50 | VDD |

| <i>J2 – PIA Connector</i> | | | |
|---------------------------|--------------------|------------|--------------------|
| <i>Pin</i> | <i>Signal Name</i> | <i>Pin</i> | <i>Signal Name</i> |
| 1 | VDD | 2 | VSS |
| 3 | CA1 | 4 | CA2 |
| 5 | PA0 | 6 | PA1 |
| 7 | PA2 | 8 | PA3 |
| 9 | PA4 | 10 | PA5 |
| 11 | PA6 | 12 | PA7 |
| 13 | NO CONNECT | 14 | NO CONNECT |
| 15 | CB1 | 16 | CB2 |
| 17 | PB0 | 18 | PB1 |
| 19 | PB2 | 20 | PB3 |
| 21 | PB4 | 22 | PB5 |
| 23 | PB6 | 24 | PB7 |
| 25 | VSS | 26 | VDD |

| <i>J3 – VIA Connector</i> | | | |
|---------------------------|--------------------|------------|--------------------|
| <i>Pin</i> | <i>Signal Name</i> | <i>Pin</i> | <i>Signal Name</i> |
| 1 | VDD | 2 | VSS |
| 3 | CA1 | 4 | CA2 |
| 5 | PA0 | 6 | PA1 |
| 7 | PA2 | 8 | PA3 |
| 9 | PA4 | 10 | PA5 |
| 11 | PA6 | 12 | PA7 |
| 13 | NO CONNECT | 14 | NO CONNECT |
| 15 | CB1 | 16 | CB2 |
| 17 | PB0 | 18 | PB1 |
| 19 | PB2 | 20 | PB3 |
| 21 | PB4 | 22 | PB5 |
| 23 | PB6 | 24 | PB7 |
| 25 | VSS | 26 | VDD |

| <i>J4 – ACIA Connector</i> | | | |
|----------------------------|--------------------|------------|--------------------|
| <i>Pin</i> | <i>Signal Name</i> | <i>Pin</i> | <i>Signal Name</i> |
| 1 | VDD | 2 | VSS |
| 3 | CA1 | 4 | CA2 |
| 5 | PA0 | 6 | PA1 |
| 7 | PA2 | 8 | PA3 |
| 9 | PA4 | 10 | PA5 |



2. Connector Descriptions

Following are descriptions of main board connectors.

2.1 XBus Port (J1)

The “XBus816” is a 50-pin male connector with the following signals:

- 8 Data Bus lines (D0-D7)
- 24 Address Bus lines (A0-A15; 64 Kbyte space)
- 3 External Chip Select Lines for expansion (XCS0B-XCS2B)
- 9 Control lines (PHI2, RWB, BE, VDA, VPA, MLB, RESB, NMIB, IRQB, VPB)
- 4 Power and Ground - 2x VSS (Pins 2 and 49) and 2x VDD (Pins 1 and 50)

2.2 PIA Port (J2)

The PIA Port Connector is an asynchronous parallel expansion port connected to the W65C21S/N. It is a 26 Pin (2 x 13; .100” spacing) male connector that provides access to the 20 I/Os (8x PA, 8x PB, CA1/2, CB1/2) of the PIA. The remaining pins serve as Power (x2) and Ground pins (x4). See section 1.4 – Quick Reference Guide for a full pin listing. Refer to the [W65C21 Datasheet](#) for detailed information for that chip.

2.3 VIA Port (J3)

The VIA Port Connector is an asynchronous parallel expansion port connected to the W65C22N. It is a 26 Pin (2 x 13; .100” spacing) male connector that provides access to the 20 I/Os (8x PA, 8x PB, CA1/2, CB1/2) of the VIA. The remaining pins serve as Power (Pins 1 and 26) and Ground pins (Pins 2, 13, 14, 35). See section 1.4 – Quick Reference Guide for a full pin listing. Refer to the [W65C22 Datasheet](#) for detailed information for that chip.

2.4 ACIA Port (J4)

The ACIA Port Connector is an asynchronous serial expansion port connected to the W65C51N. It is a 10 Pin (2 x 5; .100” spacing) connector that provides access to the 8 communication signals of the ACIA. Pin 1 is VDD and Pin 2 is VSS. See section 1.4 – Quick Reference Guide for a full pin listing. Refer to the [W65C51 Datasheet](#) for detailed information for that chip.

2.5 Micro USB TIDE Port (J5)

The Micro USB connector is dual purpose. It is the power connector that powers the board. The FTDI chip that interfaces to the connector has been pre-programmed so that when the board is power from a USB power on a computer, the chip will request 500mA of current from the host machine. The board can also be powered by any USB port that supplies 5V DC. Note that the board does not have a voltage regulator. 5V DC must be supplied. In addition to the power, the USB port serves as an interface to WDC’s tool suite for debugging and loading programs into the onboard SRAM.



3 Notices and Ordering Information

3.1 FCC Compliance

The Western Design Center, Inc. (WDC) provides the enclosed product under the following conditions: This board is intended for use for Engineering Development or Evaluation Purposes ONLY and is not considered by WDC to be a finished consumer product. This board should be handled with caution using good electronics handling practices. This board is compliant per RoHS/Green directives. It does not fall within the scope of directives such as FCC, CE, and UL. It generates uses and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules.

3.2 Ordering Information

The W65C816SXB will be available through various distributors. For information about WDC's distribution channels, please visit: <http://65xx.com/distributors/>